IN THE CLAIMS

1. – 19. (Cancelled)

20. (Currently Amended) A method for operating a memory device comprising:

receiving a sector erase command defining a sector erase operation, said sector erase operation comprising six cycles, wherein said sector erase command is issued during a third cycle of said sector erase operation;

during a first time period, issuing said sector erase command at a first data storage bank;

receiving a burst read command defining a burst read operation; and during a second time period, issuing said burst read command at a second data storage bank, wherein said first time period and said second time period overlap.

21. (Cancelled)

22. (Currently Amended) The method of Claim [[21]] <u>20</u>, wherein said burst read operation comprises four cycles, wherein said burst read command is issued during said third cycle of said burst read operation.

AMD-E0471.CON/JPH/MJB Examiner: Nguyen, Hiep T.

23. (Previously Presented) The method of Claim 22, wherein said sector erase operation further comprises initiating an unlock register command at a first cycle and a second cycle.

24. (Previously Presented) The method of Claim 23, wherein said sector erase operation further comprises initiating said unlock register command at a fourth cycle and a fifth cycle.

25. (Previously Presented) The method of Claim 24, wherein said sector erase operation further comprises initiating a sector address command at a sixth cycle.

26. (Previously Presented) The method of Claim 23, wherein said burst read operation further comprises initiating said unlock register command at said first cycle and said second cycle.

27. (Previously Presented) The method of Claim 24, wherein said burst read operation further comprises enabling the burst read command at said fourth cycle.

28. (Currently Amended) A memory device comprising:

a first bank of data storage cells;

a second bank of data storage cells; and

a state machine coupled to said first bank and said second bank, said state machine configured to initiate a sector erase command of an embedded sector erase operation at said first bank during a third clock cycle of said sector erase operation while initiating a burst read command of an embedded burst read operation during said third clock cycle of said burst read operation.

- 29. (Cancelled)
- 30. (Cancelled)
- 31. (Previously Presented) The memory device of Claim 28 wherein said state machine comprises:
 - a front end to decode user commands; and
- a back end to control embedded operations in response to said user commands.
- 32. (Previously Presented) The memory device of Claim 31 wherein said front end is configured to decode said burst read command and said back end is configured to control said sector erase command.
- 33. (Previously Presented) The memory device of Claim 31 wherein said front end is configured to permit execution of a predetermined

subset of said user commands, wherein said predetermined subset comprises said burst read command.

34. (Currently Amended) A method for operating a flash memory, the method comprising:

in response to a received sector erase command, initiating an embedded sector erase operation of a first data storage bank of said flash memory during a third cycle of said sector erase operation, wherein said sector erase operation comprises six cycles, said embedded sector erase operation comprising initiating said sector erase command; and

concurrent to said initiating said sector erase command, in response to a received burst read command, initiating a burst read operation of a second data storage bank of said flash memory during said initiating said sector erase command, said burst read operation comprising initiating said burst read command.

35. (Cancelled)

36. (Currently Amended) The method of Claim [[35]] 34, wherein said burst read operation comprises four cycles, wherein said initiating said burst read command is issued during said third cycle of said burst read operation.

AMD-E0471.CON/JPH/MJB Serial No.: 10/603,136 Examiner: Nguyen, Hiep T. - 5 -Group Art Unit: 2187

37. (Previously Presented) The method of Claim 36, wherein said sector erase operation further comprises initiating an unlock register command at a first cycle and a second cycle.

38. (Previously Presented) The method of Claim 37, wherein said sector erase operation further comprises initiating said unlock register command at a fourth cycle and a fifth cycle.

39. (Previously Presented) The method of Claim 38, wherein said sector erase operation further comprises initiating a sector address command at a sixth cycle.

- 40. (Previously Presented) The method of Claim 37, wherein said burst read operation further comprises initiating said unlock register command at said first cycle and said second cycle.
- 41. (Previously Presented) The method of Claim 38, wherein said burst read operation further comprises enabling the burst read command at said fourth cycle.

Serial No.: 10/603,136 Group Art Unit: 2187